**[Programmable Communication Group](https://sites.google.com/a/temple.edu/programmable-communication-group/)**

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| Date | Friday, September 13, 2013 | | |
| Advisor | Dr. Silage | | |
| Members | Cedric Destin | Brandon Keith | Brian Thibodeau |

Headline: WebEx project review for 9/20/13 has been dismissed, but 10/4/13 is still firm. Get familiar with WebEx. Brandon will be the first WebEx presenter.

Topics to discuss

* Demonstrate the system-level Simulink model of KD2BD modem (w/o AFC or AGC).
* Access to Xilinx LogiCore blocks in System Generator library (in Silage lab).
* Can we start assigning monthly task for the Webex?

Dr. Silage feedback

* Explained how the transmitting was done in the 90’s using a small deviation (3.5kHz) phase modulation was accomplished to transmit signals.
  + The reason why this was done was because old radio transmitters did not have on board phase madulators
* Ensure that the simulation times throughout Simulink models are realistic (i.e. 1/1200 for 1200 bps).
* Let’s choose one way of converting sinusoids to square waves throughout the Simulink models. We should either use sign/zero-order hold method or comparator (or other method).
  + I (Brian) suggest we use Dr. Silages method of a sign block used in conjunction with a rate transition.
* Doppler shift (frequency shifting) could be implemented by using a VCO with a slowly oscillating voltage input.
* Brian: possibly convert the output of your phase detector to a square wave. Refrain from doing it if it doesn’t conform to the functionality of the design (i.e. square wave may work in the presence of no noise, but what about when noise is introduced?)
* In general, convert sinusoids throughout KD2BD design to square waves as soon as possible. Don’t convert if it doesn’t conform to the functionality of the design however.

Topics to discuss in next SD meeting

* Clarify Dr. Silage’s understanding of phase detector output
* Pick a Project category out of the four categories suggested by Dr. Silage
  + Category 1. Projects sponsored  and supported by industrial partners
  + Category 2. Projects sponsored  and supported by Faculty with active research agenda
  + Category 3. Projects based on national competitions and sponsored  and supported by the Departments and College
  + Category 4. Projects originated by students without industry or Faculty support

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| **Engineer** | **Status** |
| Brian Thibodeau | * Modifying carrier recovery circuit IAW with Dr. Silage Feedback (i.e. signal conversion to square wave, PM modulator, realistic timings).   + Projected completion: Tues 9/17 * Add AWGN to carrier recovery module. Once module has been demonstrated to work in presence with noise, add attenuation so that AGC can simulated.   + Projected Completion: Mon 9/22 |
| Cedric Destin | * [Priority] Integrating the Simulink Model of the modem   + Analyze the modulated data (Is it SSB if yes why?)   + Synchronize the NRZI out * Analyzing the modem in the temporal and frequency domain   + I will use the time scope and frequency analyzer |
| Brandon Keith | * No notable progress has been made since SD meeting on 9/6/13. Tasks remain the same as 9/6/13. I didn't work on SD this week. |